**What is claimed is:**

1. A source driver in a liquid crystal display apparatus for receiving an input voltage and generating an output voltage to drive a data line, comprising:

a ground terminal to which a ground voltage is applied;

a power supply terminal to which a power supply voltage higher than the ground voltage is applied;

an input terminal for receiving the input voltage;

an output terminal for generating the output voltage;

first and second P-channel MOS transistors each having a gate connected to a drain of the first P-channel MOS transistor, the second P-channel MOS transistor having a source connected to the output terminal;

first and second N-channel MOS transistors each having a gate connected to a drain of the first N-channel MOS transistor, the second N-channel MOS transistor having a source connected to the output terminal;

a third N-channel MOS transistor having a gate connected to the input terminal and a source connected to a source of the first P-channel MOS transistor;

a third P-channel MOS transistors having a drain connected to the power supply terminal, and a gate connected to a source of the third P-channel MOS transistor;

a first switch connected between the source of the third P-channel MOS transistor and the drain of the first N-channel MOS transistor;

a second switch connected between the ground terminal and the drain of the first P-channel MOS transistor;

a third switch connected between the power supply terminal and a drain of the third N-channel MOS transistor;

a fourth switch connected between the input terminal and a source of the first N-channel MOS transistor;

a fifth switch connected between the power supply terminal and a drain of the second N-channel MOS transistor;

a sixth switch connected between the ground terminal and a drain of the second P-channel MOS transistor; and

a first capacitor connected between a control signal terminal and the drain of the first N-channel MOS transistor.

2. The source driver as claimed in claim 1, wherein the first capacitor is operated to boost the voltage of the drain of the first N-channel MOS transistor on the level of at least the input voltage plus the threshold voltage of the N-channel MOS transistor at a predetermined time.

3. The source driver as claimed in claim 1, wherein the third and second switches are operated to bias the gate of the second P-channel MOS transistor a voltage of (Vin+Vthp1-Vthn3) at a predetermined time, Vin being the input voltage, Vthp1 being a threshold voltage of the first P-channel MOS transistor, Vthn3 being a threshold voltage of the third N-channel MOS transistor.

4. The source driver as claimed in claim 1, wherein the fourth and first switches are operated to bias the gate of the second N-channel MOS transistor a voltage of (Vin+Vthn1) at a predetermined time, Vin being the input voltage, Vthn1 being a threshold voltage of the first N-channel MOS transistor.

5. The source driver as claimed in claim 1, wherein the sixth switch is operated to operate the second P-channel MOS transistor as a source follower.

6. The source driver as claimed in claim 1, wherein the fifth switch is operated to operate the second N-channel MOS transistor as a source follower.

7. The source driver as claimed in claim 1, further comprising a fourth N-channel MOS transistor having a source connected to the drain of the second P-channel MOS transistor and a drain connected to the output terminal, wherein the fourth N-channel MOS transistor is used to substantially pull the output voltage to ground at predetermined time when the input voltage is smaller than the threshold voltage of the transistor.

8. The source driver as claimed in claim 1, further comprising:

a fourth P-channel MOS transistor having a gate connected to the input terminal and a source connected to the source of the first N-channel MOS transistor; and

a seventh switch connected between the ground terminal and a drain of the fourth P-channel MOS transistor.

9. The source driver as claimed in claim 8, further comprising a ninth switch connected between the input terminal and a source of the third N-channel MOS transistor.

10. The source driver as claimed in claim 9, wherein while the fourth and ninth switches are kept turned OFF and ON respectively, and then the fifth and sixth switches are turned ON and OFF respectively, to operate the second N-channel MOS transistor as a source follower.

11. The source driver as claimed in claim 10, wherein after the fifth and sixth switches are turned ON and OFF respectively for a predetermined period, and then the fifth and sixth switches are turned OFF and ON respectively, to operate the second P-channel MOS transistor as a source follower.

12. The source driver as claimed in claim 9, wherein while the fourth and ninth switches are kept turned ON and OFF respectively, and then the fifth and sixth switches are turned OFF and ON respectively, to operate the second P-channel MOS transistor as a source follower.

13. The source driver as claimed in claim 12, wherein after the fifth and sixth switches are turned OFF and ON respectively for a predetermined period, and then the fifth and sixth switches are turned ON and OFF respectively, to operate the second N-channel MOS transistor as a source follower.

14. The source driver as claimed in claim 9, further comprising a eighth switch connected between the input terminal and the output terminal, the eighth switch being turned ON after operation of the second P-channel MOS transistor or the second N-channel MOS transistor as a source follower.

15. The source driver as claimed in claim 9, further comprising a fourth N-channel MOS transistor having a source connected to the drain of the second P-channel MOS transistor and a drain connected to the output terminal, wherein the fourth N-channel MOS transistor is used to substantially pull the output voltage to ground at predetermined time when the input voltage is smaller than the threshold voltage of the transistor.

16. The source driver as claimed in claim 9, further comprising a fifth N-channel MOS transistor and a fifth P-channel MOS transistor, wherein the fifth N-channel MOS transistor has a source connected to the output terminal, a drain connected to the power supply terminal, and a gate connected to the input terminal, and the fifth P-channel MOS transistor has a source connected to the output terminal, a drain connected to the ground terminal, and a gate connected to the input terminal.

17. The source driver as claimed in claim 1, wherein, after the gate of the second P-channel MOS transistor is biased on the voltage level of (Vin-Vthn3+Vthp1), the sixth and fifth switches are turned ON and OFF, respectively, to operate the second P-channel MOS transistor as a source follower Vin being the input voltage, Vthp1 being a threshold voltage of the first P-channel MOS transistor, Vthn3 being a threshold voltage of the third N-channel MOS transistor.

18. The source driver as claimed in claim1, wherein, after the gate of the second N-channel MOS transistor is biased on the voltage level of (Vin+Vthn1), the sixth and fifth switches are turned OFF and ON, respectively, to operate the second N-channel MOS transistor as a source follower, Vin being the input voltage, Vthn1 being a threshold voltage of the first N-channel MOS transistor.

19. The source driver as claimed in claim 1, further comprising a eighth switch connected between the input terminal and the output terminal, the eighth switch being turned ON after operation of the second P-channel MOS transistor or the second N-channel MOS transistor as a source follower.

20. The source driver as claimed in claim 1, further comprising a fifth N-channel MOS transistor and a fifth P-channel MOS transistor, wherein the fifth N-channel MOS transistor has a source connected to the output terminal, a drain connected to

the power supply terminal, and a gate connected to the input terminal, and the fifth P-channel MOS transistor has a source connected to the output terminal, a drain connected to the ground terminal, and a gate connected to the input terminal.